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Question Paper Code : 71464

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Eighth/Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64/10144 EC 704 — VLSI DESIGN

(Common to Biomedical Engineering)

(Regulation 2008/2010)

(Common to PTEC 2354 — VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the DC transfer characteristics of CMOS inverter.

2. Define lambda based design rules used for layout.

3. State the types of power dissipation.

4. Define Scaling. What are the advantages of scaling?

5. Implement a 2:1 Mux using pass transistor.

6. Design a one transistor DRAM cell.

7. State the need for testing.

8. State the principle behind manufacturing testing.

9. State the operators used in Verilog HDL.

10. Write a Verilog program for a CMOS inverter using switch level modelling.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the DC transfer characteristics of CMOS inverter.

Or

(b) Explain in detail with neat diagram the steps involved in the fabrication of nwell process.

12. (a) (i) Explain the various techniques to reduce static and dynamic power dissipation. (10)

(ii) Derive an expression for the nMOS inverter pair delay whose transistor size is 4:1. (6)

Or

(b) Derive an expression for the rise time, fall time and propagation delay of a CMOS inverter.

13. (a) (i) Implement a XOR gate using CMOS logic. (8)

(ii) Compare CMOS, Dynamic, Domino and Pseudo nMOS logic families. (8)

Or

(b) (i) Design a d-latch using transmission gate. (8)

(ii) Design a 1-bit Dynamic inverting and Non-inverting Register using pass transistor. (8)

14. (a) Explain Boundary Scan testing.

Or

(b) Explain logic verification in detail.

15. (a) Explain how to represent the gate delays in Verilog HDL with an example.

Or

(b) (i) Write a Verilog code for D-flip-flop. (8)

(ii) Explain blocking and non-blocking assignments. (8)